Curriculum Vitae
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TakaHide Ohkami

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Citizenship: USA – Naturalized in February 2015
Languages: English, Japanese (native), Spanish (learning)

PROFESSIONAL INTERESTS

Computer architecture, computer hardware design with VHDL, Verilog, and SystemC, programming in C, C++, C#, Python, Java, Lisp, and Assembler, compilers and assemblers, operating systems, computer algorithms, computing system issues, and problem solving.

PROFESSIONAL SUMMARY

Teaching Electrical and Computer Engineering Courses
- Lecture and laboratory classes on digital electronics, hardware design with VHDL, programming in C and assembly, microcomputers/microcontrollers, embedded systems, and software development with Java.

Embedded Software/Firmware Design, Evaluation, and Testing
- Real-time, digital, mixed-signal, signal processing, image processing, etc.
- Programming in C/C++/C#/Python with real-time operating systems

ASIC/FPGA RTL Design, Evaluation, and Verification
- Digital logic design in Verilog and verification with Cadence and Synopsys tools
- Silicon evaluation with C and C++

Hardware/Software System Engineering
- System evaluation, analysis, modeling, and troubleshooting
- International/domestic multi-site project coordination
- Technical problem-solving for international automotive and non-automotive customers

EDUCATION

Ph.D.	in Computer Engineering	University of Tokyo, Tokyo, Japan (1992)
M.S.	in Computer Science	University of Rochester, Rochester, NY (1987)
B.E.	in Control Engineering	University of Tokyo, Tokyo, Japan (1977)

APPLICATION AREAS OF EXPERIENCE

- Electrical and Computer Engineering Course Teaching
- Wearable embedded systems at Radiation Monitoring Devices
- Hall-effect based current/linear/angle sensor ICs at Allegro MicroSystems
- BLURAY chips and systems at Broadcom
- 3D graphics (texture mapping) at AMD (Advanced Micro Devices)
- Electronic book readers (Kindle and others) at E-Ink
- Flash memory at Mobile-Mind
- Parallel image processing DSP-based ICs at ChipWrights
- Hardware accelerators for HDL simulations and compilers at Quickturn/Cadence
- Various computing hardware and software systems at Mitsubishi Electric

WORK EXPERIENCE

Lecturer
University of New Hampshire at Manchester (January 2022 – Present)
- COMP730/830 (Software Development) Spring 2024, Fall 2023, Spring 2023, Fall 2022, Spring 2022
- GRAD900 (Master's Continuing Project/Thesis) Spring 2024
- COMP898/890 (Master's Project/Thesis) Fall 2023
- ET730/830 (Software Development) Fall 2022
- ET790 (Microcomputer Technology) Fall 2023, Fall 2022
- ET590 (Embedded Microcontrollers) Spring 2023, Spring 2022
- ET522 (Digital Electronics II) Spring 2022
- ET421 (Digital Electronics I) Spring 2024, Spring 2022

Adjunct Faculty
University of New Hampshire at Manchester (August 2020 – December 2021)
- ET791/751 (Electrical/Mechanical Engineering Technology Project) Spring 2021, Fall 2020
- ET790 (Microcomputer Technology) Fall 2021, Fall 2020
- ET522 (Digital Electronics II) Fall 2021
- ET421 (Digital Electronics I) Spring 2021

Embedded Software Engineer (Part-Time Contractor)
Radiation Monitoring Devices, Watertown, MA (April 2020 – January 2023)
- Developed ARM-based embedded system firmware modules with C, Python, and FreeRTOS.

Principal System Engineer
Allegro MicroSystems, Manchester, NH (September 2011 – March 2020)
- Performed silicon evaluation of Hall-effect-based angle sensor ICs with MATLAB and Python.
- Analyzed large production data with MATLAB, Ruby, Python, and C#.
- Designed and verified FPGA (Xilinx, ATMEL) for sensor programming with Verilog, SystemVerilog.
- Designed and verified firmware and user interface software in C/C++/C# for sensor programming.
- Provided technical support for automotive and non-automotive customers in USA, Japan, and Europe.

Scientist - Firmware
Broadcom, Andover, MA (December 2010 – September 2011)
- Developed and verified the BLURAY chip initialization and memory test codes in C/C++.
- Verified the BLURAY chip functions and performance using C/C++.

Senior Member of Technical Staff (ASIC/Emulator Design/Verification)
Advanced Micro Devices (AMD), Boxborough, MA (April 2008 – November 2010)
- Designed and verified the new functions of the texture data and address units in C++/Verilog/SystemVerliog.

Staff System Engineer (FPGA/ASIC Design Engineer), Project Lead (System Design)
E Ink Corporation, Cambridge, MA (May 2005 – April 2008)
- Designed a new ASIC controller architecture and chip structure for a chip manufacturer.
- Designed and verified FPGA controller chips for electronic paper display panels in Verilog and System Verilog.
- Designed and verified the Linux device driver in C for display controllers.
- Provided technical support for Japanese customers.
- Solved the memory bus data stream interruption problems with a customer.

Senior Technical Advisor (Hardware/Software R&D Engineer)
Mobile-Mind, Watertown, MA (December 2004 – May 2005)

- Investigated the hardware-based software protection technologies with flash memories in C/C++.
- Managed the R&D collaboration with a Spansion flash memory team in Japan.

Consulting Engineer (ASIC Design/Verification Engineer)
ChipWrights, Inc., Waltham, MA (December 2000 – September 2004)

- Developed several parallel DSP chips (1-2M gates + SRAMs) at 200-333 MHz with Verilog.
- Developed C++ programs for DDR-SDRAM interface, AMBA AHB system, and video/audio interfaces.
- Developed a new DDR-SDRAM prefetching scheme for different data streams.
- Developed C++ programs to model/analyze DSP functionality and performance for image/video processing.
- Developed device drivers in C, C++, and assembly for FLASH memories, SD cards, and other I/O devices.
- Provided customer support for solving design problems with the DSP chips.

Senior Member of Consulting Staff (Software Engineer)
Quickturn (a Cadence Company), Lowell, MA (June 1999 – December 2000)

- Developed C++ programs to enhance the logic simulator product (PowerSuite) with the hardware accelerators.
- Developed a packet-based interface for the hardware logic simulation accelerator CoBALT.
- Developed parallel sorting algorithms in C++ to evaluate the hardware logic simulation accelerators.
- Provided customer support for the logic simulation with the hardware logic simulation accelerators.

Senior Research Staff, R&D Manager
Mitsubishi Electric Information Technology Center America, Cambridge, MA (April 1991 – June 1999)

- Contributed to the design of a real-time volume graphics chip by the development of several simulators.
- Developed an algorithmic simulator in C++ to generate the volume-rendered images.
- Developed a cycle-accurate simulator in C++ for the volume rendering pipeline structure.
- Developed the Verilog modules using the cycle-accurate simulator.
- Developed the verification method of the final images rendered by the chip using the algorithmic simulator.
- Performed the mathematical analysis of the images generated by the volume rendering algorithm.
- Explored a parallel-pipeline volume rendering architecture for both parallel and perspective projections.
- Provided customer support for the volume rendering architecture and system.
- Evaluated various irregular volume rendering methods.
- Investigated the modular display system to support 10-100 million pixels on a tiled screen.
- Coordinated R&D activities between USA and Japan.
- Performed various administrative tasks to establish a U.S. research laboratory in Cambridge, MA.

R&D Engineer, R&D Assistant Manager
Mitsubishi Electric Corporation (R&D Laboratories), Kamakura, Japan (April 1977 – March 1991)

- Analyzed the online transaction processing system with SQL for performance enhancement.
- Prototyped the parallel programming tools in C for performance analysis/debug tools.
- Investigated the advanced features of vectorizing/parallelizing compilers.
- Learned parallel programming of BBN Butterfly at the University of Rochester (Computer Science Department).
- Designed a 32-bit DSP chip architecture for image processing.
- Designed a Prolog-based inference machine in the Japanese Fifth-Generation Computer Project.
- Designed a VLIW-like architecture for a real-time radar signal processor optimized for FFT and filter operations.
- Designed several modules for a general-purpose ECL computer.
- Investigated the ECL gate array chip structure.
- Designed a 16-bit minicomputer CPU board with 600-gate NMOS gate array chips.
- Transferred to the USA technology center in Cambridge, MA.

TECHNICAL PUBLICATIONS (25)

- H. Gates, T. Ohkami, and J. Au, “Improved Electronic Controller for Image Stable Displays,” Proc. SID (Society for Information Display), ’06 Conf., June 2006, Paper No. 37.2.
- H. G. Gates, R. W. Zehner, T. Ohkami, and D. Bischoff, “Low-Power Displays for Mobile Devices,” Proc. Americas Display Engineering & Applications Conf., October 2005, Paper No. 11.1.
- M. Ogata, T. Ohkami, H. Lauer, and H. Pfister, "A Real-Time Volume Rendering Architecture Using an Adaptive Resampling Scheme for Parallel and Perspective Projections," Proc. 1998 Symp. Volume Visualization, Oct. 1998, pp.31-38.
- S. Gibson, C. Fyock, E. Grimson, T. Kanade, R. Kikinis, H. Lauer, N. McKenzie, A. Mor, S. Nakajima, H. Ohkami, R. Osborne, J. Samosky, and A. Sawada, "Volumetric Object Modeling for Surgical Simulation," Medical Image Analysis, Vol.2, No.2, 1998, pp.121-132.
- R. Osborne, H. Pfister, H. Lauer, N. McKenzie, S. Gibson, W. Hiatt, and T. Ohkami, "EM-Cube: An Architecture for Low-Cost Real-Time Volume Rendering," Proc. 1997 SIGGRAPH/Eurographics Work. Graphics Hardware, Aug. 1997, pp.131-138.
- S. Gibson, J. Samosky, A. Mor, C. Fyock, E. Grimson, T. Kanade, R. Kikinis, H. Lauer, N. McKenzie, S. Nakajima, H. Ohkami, R. Osborne, and A. Sawada, "Simulating Arthroscopic Knee Surgery Using Volumetric Object Representations, Real-Time Volume Rendering and Haptic Feedback," Proc. 1st Joint Conf. Computer Vision, Virtual Reality and Robotics in Medicine and Medical Robotics and Computer-Assisted Surgery, Mar. 1997, Lecture Notes in Computer Science, Vol.1205, Springer-Verlag, pp.369-378.
- T. Ohkami, "Intelligent Displays: Displaying the Network," Information Display, Jan. 1997, pp.14-16.
- T. Ohkami, "Modular Display: An Approach to Intelligent Display Systems," Proc. SID (Society for Information Display) '96 Conf., May 1996, pp.225-228.
- T. Ohkami, "Dynamically Reconfigurable Architecture for a Class of Real-Time Applications," Ph.D. Thesis, Department of Mathematical Engineering and Instrumentation Physics, University of Tokyo, January 1992.
- T. Matsuzawa, N. Ogawa, T. Ohkami, and T. Noji, "An OLTP Performance Prediction Tool: SMART," Proc. 1991 Spring IPS Japan Nat'l Conf., Vol.4, Mar. 1991, pp.73-74. (in Japanese)
- N. Ogawa, Y. Yamanaga, T. Matsuzawa, T. Ohkami, and T. Noji, "Performance Analysis of OLTP Systems Using the TPC Model," Proc. Operating Systems Meet. IPS Japan, Mar. 1991, Paper No.50-2. (in Japanese)
- T. Ohkami, "A Unified Approach to Debugging and Performance Evaluation of Parallel Programs," Proc. Programming Language Meet. IPS Japan, Feb. 1988, Paper No.15-1.
- T. Ohkami, "Experience with Chrysalis/Butterfly," Proc. Operating Systems Meet. IPS Japan, Dec. 1987, Paper No.37-5.
- T. Ohkami, "PARPAT: Parallel Performance Analysis Tools," Technical Memo, Department of Computer Science, University of Rochester, Apr. 1987.
- T. Ohkami and D. Bouldwin, "The SEEDS (Simulator for Experimental Electronic Design Systems) Simulator: User Manual and Report (Version 1.0)," Technical Memo, Department of Computer Science, University of Rochester, Aug. 1986.
- T. J. LeBlanc, N. M. Gafter, and T. Ohkami, "SMP: A Message-Based Programming Environment for the BBN Butterfly," Butterfly Project Report No.8, Department of Computer Science, University of Rochester, Jul. 1986.
- S. Tsujimichi, T. Ohkami, and Y. Shimazu, "A Next-Generation 32-Bit VLSI Signal Processor," Proc. IEEE-IECEJ-ASJ Int'l Conf. Acoustics, Speech, and Signal Processing, Apr. 1986, pp.413-416.
- T. Ohkami, M. Furuichi, and K. Taki, "Sequential Inference Machine PSI -- System Control and RAS," Proc. 1984 Fall IPS Japan Nat'l Conf., Oct. 1984, pp.57-58. (in Japanese)
- T. Ohkami, "MSP: A High-Speed Signal Processor with a Dynamically Reconfigurable Computation Network," Proc. 1984 Int'l Symp. Noise and Clutter Rejection in Radars and Imaging Sensors, Oct. 1984, pp.633-638.
- T. Ohkami and A. Iwase, "An Architecture of a Small Control Processor for High-Speed Real-Time Signal Processing," Proc. IEEE COMPCON '84 Fall Conf., Sep. 1984, pp.255-262.
- T. Ohkami, "A Signal Processor with a Dynamically Reconfigurable Computation Network," Proc. Information Processing Group Meet. IEE Japan, Nov. 1983, Paper No.IP-83-41. (in Japanese)
- T. Ohkami, A. Iwase, and C. Tanaka, "An Evaluation on the Functionality of the Series-Gate Cell for the ECL Gate Array," Proc. 1983 Spring IECE Japan Nat'l Conf., Apr. 1983, Paper No.1591. (in Japanese)

- T. Ohkami, A. Iwase, and C. Tanaka, "Pipelined FFT Processing," Proc. 1982 Fall IPS Japan Nat'l Conf., Oct. 1982, pp.161-162. (in Japanese)
- T. Ohkami, N. Iijima, T. Sakamoto, T. Hirai, A. Iwase, and C. Tanaka, "A Dynamically Reconfigurable Computation Network for Flexible and High-Speed Signal Processing," Proc. IEEE Int'l Conf. Circuits and Computers, Sep.-Oct. 1982, pp.52-55.
- H. Matsushita, T. Ohkami, T. Ogiwara, and S. Murai, "Maximum Matching in a Graph Whose Vertices' Interconnections Are Defined by Their Types," Trans. IECE Japan, Vol.J65-A, No.8, Aug. 1982, pp.842-848. (in Japanese)

PATENTS (23)

- Y. S. Low, J. P. van Baarsen, and T. Ohkami, Time-Overlapping Partial-Panel Updating of a Bistable Electro-Optic Display, U.S. Patent Application 20090256868, October 2009.
- T. Ohkami and H. G. Gates, *Methods for Driving Electro-Optic Displays*, U.S. Patent Application 20090256799, October 2009.
- T. Ohkami and John Redford, *Memory Control System and Method In Which Prefetch Buffers Are Assigned Uniquely to Multiple Burst Streams*, U.S. Patent Application 20050253858, November 2005.
- T. Ohkami, *Hardware-Assisted Design Verification System Using a Packet-Based Protocol Logic Synthesized for Efficient Data Loading and Unloading*, U.S. Patent 7054802, 5/30/06.
- J. Knittel, K. Correll, J. Hardenbergh, C. Kappler, H. Lauer, S. Mason, W. Peet, B. Schultz, J. Wilkinson, S. Burgess, T. Ohkami, and H. Pfister, *Volume Rendering Pipeline*, U.S. Patent 6532017, 3/11/03.
- J. Knittel, K. Correll, J. Hardenbergh, C. Kappler, H. Lauer, S. Mason, W. Peet, B. Schultz, J. Wilkinson, S. Burgess, T. Ohkami, and H. Pfister, *Volume Rendering Integrated Circuit*, U.S. Patent 6512517, 1/28/03.
- M. Ogata, T. Ohkami, and H. Lauer, *Parallel Volume Rendering System with a Resampling Module for Parallel and Perspective Projections*, U.S. Patent 6313841, 11/6/01.
- T. Ohkami, *Data Formatting System for Processing Multiple Independent Input Data Streams for High Resolution Screen Displays*, U.S. Patent 5754242, 5/19/98.
- T. Ohkami, *Computer Program Version Management System with Reduced Storage Space and Enabling Multiple Program Versions to Have the Same Name*, U.S. Patent 5603027, 2/11/97.
- T. Ohkami, *Scaleable Very Long Word Processor with Parallelism Matching*, U.S. Patent 5600810, 2/4/97.
- A. Ishizuka and T. Ohkami, *Compiling System for Distributed Computer System with Multiple Types of Computer*, U.S. Patent 5313635, 5/17/94 and Japanese Patent 2665089, 10/22/97.
- T. Ohkami, *Memory Access Method and System*, U.K. Patent 2241800, 12/8/93, U.S. Patent 5446862, 8/29/95 (Continuation U.S. Patent 5579505, 11/26/96), Japanese Patent 2665813, 10/22/97
- T. Ohkami, *Data Processing System for Array Computation*, Japanese Patent H05-61675, 9/6/93.
- T. Ohkami, *Data Processing System for Array Computation*, Japanese Patent H03-46862, 7/17/91.
- T. Matsuzawa and T. Ohkami, *Method and System for File Access*, Japanese Patent Application, 1/11/91.
- T. Matsuzawa and T. Ohkami, *Method for I/O Control of Computers*, Japanese Patent Application, 8/7/90.
- T. Kawada and T. Ohkami, *Method for Program Execution*, Japanese Patent Application H03-252856, 3/2/90.
- T. Ohkami, N. Iijima, T. Sakamoto, and T. Hirai, Data *Processing System for Array Computation*, U.S.Patent 4825359, 4/25/89 and Japanese Patent H03-6545, 1/30/91.
- T. Ohkami, *Method for Automatic Generation of Dated Files*, Japanese Patent Application H02-278350, 4/19/89.
- T. Ohkami, *Apparatus for Microprogram Sequence Control*, Japanese Patent H01-15091, 3/15/89.
- T. Ohkami, *Parallel Computing System*, Japanese Patent Application H02-77870, 10/28/88.
- T. Ohkami and Y. Taguchi, *Method for Instruction Buffer Control*, Japanese Patent S62-11736, 3/14/87.
- T. Ohkami, *3-Dimensional Interconnection Method of IC Chips*, Japanese Patent S60-19664, 5/17/85.

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