UNH Materials Science Seminar

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Epitaxial Oxide Growth on Si(001) for Floating Epitaxy, a Novel Process for Silicon-on-Insulator Wafer Production

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As scaling continues in the semiconductor industry, silicon-on-insulator (SOI) wafers are increasingly becoming the substrate of choice, due to higher channel mobility, effective device isolation, reduced short channel effects, minimized parasitic capacitance, and therefore higher speed, compared to a regular silicon wafer. Current methods of SOI wafer production, however, will have difficulty achieving the desired silicon device layer and buried oxide insulator layer thicknesses and eliminating interface roughness as scaling proceeds. We propose “Floating Epitaxy SOI” as a novel method of SOI production utilizing an all *in-situ* growth process. Floating Epitaxy SOI involves Molecular Beam Epitaxy deposition of an epitaxial template oxide, oxidizing through the epitaxial template layer to establish the insulation layer, and silicon growth on top of the epitaxial template oxide layer (which is now “floating” on top of an amorphous oxide layer). The key to this process is the epitaxial oxide template layer, which must deposit on the silicon substrate as an atomically smooth film with a lattice parameter close to that of silicon and must be sufficiently

stable in both oxygen and vacuum annealing to relatively high temperature to achieve Floating Epitaxy SOI. Although many researchers have examined epitaxial oxides on silicon, this study focuses on epitaxial films over large area substrates, while virtually all other studies report on growth on small substrate sizes. Also, the oxide stability limits on silicon in vacuum have not been thoroughly established by previous work, and are investigated here. The growth and thermal stability of this epitaxial oxide template layer are discussed, as well as brief results for through-oxidation "floating" of the template oxide layer and silicon growth experiments.

Jennifer Hydrick is a Staff Scientist and member of the engineered substrate research group at AmberWave Systems in Salem, NH, focusing on chemical-mechanical planarization process development for germanium and other semiconductor materials. Jennifer received her B.S. in Materials Science Engineering from Alfred University, where she investigated the viability of PMN-PEEK piezocomposites. She earned her M.S. in Materials Science Engineering from North Carolina State University doing research on a novel method of Silicon-on-Insulator (SOI) wafer creation, called Floating Epitaxy SOI, which involves Molecular Beam Deposition of an epitaxial oxide template material lattice-matched to silicon as the basis of the silicon device layer deposition. Jennifer is a member of the Society of Women Engineers and the Materials Research Society.